Attorney's Docket No.: 08305/069001/99-07

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: MULTI JUNCTION APS WITH DUAL SIMULTANEOUS INTEGRATION

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MULTIPLE JUNCTION ACTIVE PIXEL SENSOR STRUCTURE WITH DUAL SIMULTANEOUS INTEGRATION

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of U.S. Provisional application No. 60/124,153, filed March 8, 1999.

BACKGROUND

Active pixel sensors are described in U.S. patent no. 5,417,215. Higher charge and efficiency from these devices is desirable. In addition, different parameters and operations can benefit from different kinds of samples. For example, a short sampling period can provide the highest amount of dynamic range, while a longer sampling period can provide better resolution. Fossum and Yadid-Pecht have described one such system and "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling, IEEE Transactions On Electronic Devices, volume 44 page 1721-1723, October 1997. In that system, two signals are obtained using two different integration intervals.

SUMMARY

The present application teaches a new pixel design with dual floating diffusion regions, each of which is separately controlled. The two regions collectively

provide dual integration, but do so in a way that increases sensitivity, allows dual dynamic range, and also provides multiple junctions for improved photocarrier detection.

DETAILED DESCRIPTION

Figure 1 shows a first embodiment which is formed by a more standard CMOS fabrication process. There is a relatively large floating diffusion capacitance, which can tend to reduce the charge conversion gain. However, this system may be easier to make due to its use of a standard CMOS process, with the floating diffusion being on the surface.

An N-type well 100 is formed in the P-type substrate 105. A first floating diffusion region 110 is a P-type floating diffusion region formed on the surface, i.e., its top surface close to or touching the active oxide region 102. The P-type floating diffusion region 110 is connected to a P-type output transistor 115 and a P-type reset transistor 120. The reset transistor 120 connects to a P+-type diffusion region 125 which is biased, for example, to the voltage level of the drain voltage.

The second floating diffusion region 130 is an N-type floating diffusion region. Note that the second floating diffusion region 120 takes up a much smaller area then the

first floating diffusion region, e.g. one fifth as much area.

The second floating diffusion region is N-type, and is connected to an N-type output transistor 135. An NMOS reset transistor 140 connects the floating diffusion region to N+ diffusion region 145, which can be connected to a supply voltage level. In this way, a P-type region is formed extending from the edge of the P-type floating diffusion 110 to the edge of the P-type diffusion 125. The N-type region, starting at floating diffusion 130, is separate from the P-type region. In addition, the N-type region can surround virtually the entire active P type region, and all of the P+ region.

This new pixel design needs two separate reset control lines, one for the NMOS reset transistor 140 and the other for the PMOS reset transistor 120. One column can be used for both output signals, e.g. with two select control lines. Alternately, two output columns can be used with one select line.

Note that since the size of the two different floating diffusion regions is different, they will store different amounts of charge. Therefore, the floating diffusion 110 can store more charge then the floating diffusion 135. Different integration periods for these two diffusion

floating regions allow a flexible saturation exposure for each element. It also facilitates obtaining a highlighted compression knee sloped light transfer curve.

A second embodiment is shown in Figure 2. In this embodiment, the P type diffusion region 200 is formed below the surface of the N-well 202. An overlying N region 215 is formed above the floating diffusion, covered by the active oxide. The N-well 202, in this embodiment, is arranged to be fully depleted. A second smaller floating diffusion region 205 is connected to the buried floating diffusion 200, and is connected to output transistor 115. In this way, there are three superimposed PN junctions: A first junction between the overlying N region area 215 and the buried floating diffusion 200. Another PN junction is formed between the bottom of the floating diffusion 215 and the N region 202. The third PN junction is between the fully depleted N region 202, and the P type substrate 105. The capacitance for the floating N type diffusion can be reduced by this structure.

Although only a few embodiments have been disclosed and detailed above, other modifications are possible. All such modifications are intended to be encompassed within the following claims, in which: